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MINISTRY OF COMMERCE & INDUSTRY,
PATENT OFFICE, DELHI BRANCH,
W - 5, WEST PATEL NAGAR,
NEW DELHI - 110 008.

I, the undersigned being an officer duly authorized in accordance with the provision of the Patent Act, 1970 hereby certify that annexed hereto is the true copy of the ***Application, Complete Specification*** *and* ***Drawing Sheets*** *filed in connection with Application for Patent No.* ***76/Del/03*** *dated* ***30th January 2003.***

Witness my hand this 30th day of December2003.

(S.K. PANGASA)
Assistant Controller of Patents & Designs

0076 DEL 03

FORM 1
THE PATENTS ACT, 1970
(39 of 1970)

30 JAN 2003

APPLICATION FOR GRANT OF A PATENT
(See Sections 5(2), 7, 54 and 135)

1. We, ***STMicroelectronics Pvt. Ltd., Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India, an Indian Company***

2. hereby declare –

   (a) that ~~I am~~/we are in possession of an invention titled **'METHOD AND SYSTEM FOR REDUCING POWER CONSUMPTION IN DIGITAL CIRCUIT USING CHARGE REDISTRIBUTION CIRCUITS'**

   (b) that the provisional / complete specification relating to this invention is filed with this application

   (c) that there is no lawful ground of objection to the grant of a patent to me/us.

3. further declare that the inventor(s) for the said inventions is/are

   i. ***Vivek NAUTIYAL****, an Indian national of Deep Villa, Balasaur, Kotdwara, District – Garhwal, India*

   ii. ***Ashish KUMAR****, an Indian national of M-17 Housing Colony, Ranchi – 834009, India*

4. We claim the priority from the application(s) filed in connection countries, particulars of which are as follows: Nil

5. We state that the said invention is an improvement in or modification of the invention the particulars of which are as follows and of which we are the applicant/patentee: NIL

6. We state that the application is divided out of ~~my~~/our application, the particulars of which are given below and pray that this application be deemed to have been filed on under section 16 of the Act. NIL

7. That ~~I am~~/we are the assignee or legal representative of the true and first inventors N.A

8. That ~~my~~/our address for service in India is as follows:
   ANAND & ANAND, Advocates
   B-41, Nizamuddin East
   New Delhi – 110 013
   Tel Nos.: (11) 24358078, 24355076, 24350360
   Fax Nos.: (11) 24354243, 24353060

DUPLICATE

9- I/We the true and first inventors of this invention or the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.

A) VIVEK NAUTIYAL an Indian National of DEEP VILLA, BALASAUR ,KOTDWARA, DISTRICT :- GARHWAL.

Signature

Dated this day of 2002

B) ASHISH KUMAR an Indian National of M-17 Housing Colony, Ranchi-834009.

Signature

Dated this day of 2002

10- that to the best of my/our knowledge, information and belief the fact and matters stated herein are correct and that there is no lawful ground of objection to grant of patent to me/us on this application.

11- Following are the attachment with the application

(a) Complete specification (3 copies)
(b) Abstract
(c) Formal drawings
(d) Power of Attorney
(e) Form 1 (in triplicate)
(f) Form 3 (in duplicate)
(g) Fee Rs. 5000/- In cash/cheque/bank draft bearing no. , date On Bank.

I/We request that a patent may be granted to me/us for the said invention.

Dated this day of 2002

Signature
STMicroelectronics Pvt. Limited

To

The Controller of Patents
The Patent Office, Delhi

02-IND-139

0076 DEL 03

Form 2

THE PATENTS ACT, 1970

30 JAN 2003

COMPLETE SPECIFICATION

[See Section 10]

METHOD AND SYSTEM FOR REDUCING POWER CONSUMPTION IN DIGITAL CIRCUIT USING CHARGE REDISTRIBUTION CIRCUITS

STMicroelectronics Pvt. Ltd., *an Indian Company, of Sector 16A, Industrial Area, NOIDA-201301, U.P., India.*

The following specification particularly describes and ascertains the nature of this invention and the manner in which it is to be performed

METHOD AND SYSTEM FOR REDUCING POWER CONSUMPTION IN DIGITAL CIRCUIT USING CHARGE REDISTRIBUTION CIRCUITS

Field of the Invention

This invention relates to a method and system for reducing power consumption in digital circuit using charge redistribution circuits.

Background of the Invention

Advancements in LSI (Large Scale Integrated) technology continuously bring about reduced transistor sizes and corresponding many-fold increase in the number of transistors that can be mounted on a single chip. However, even though power supply voltage has been lowered considerably, the combination of size and transistor count is such that chip power consumption continues to grow resulting in increased concern with power consumption and dissipation. Power consumption and dissipation concerns have become a limiting factor in the design of LSIs used in microprocessors and other devices that require large-scale, high-speed processing. Thus, reducing power consumption has become a major priority throughout the field of LSI-related development, ranging from computer systems to circuit and device technologies.

Attempts to limit power consumption while reducing power source voltage that have been made so far have however resulted in a decline in transistor drive capability resulting in reduced operating speed. This trade off is not generally acceptable. As a result, there is a pressing need for circuit technology that can reduce energy consumption as well as source voltage without sacrificing operating speed.

Charge recycling provides a mechanism that offers a solution by utilizing charge stored in the distributed capacitance of one or more circuit nets to charge other nets that are at an opposing potential, during intermediate idle periods. This process of charge equalization, allows for a mutual exchange of energy when the data lines are transitioning thereby effectively enabling reuse of electrical power – and consequent reduction in overall power consumption.

Existing methods of charge redistribution are capable of operating with dual rail charge redistribution systems, in which paired complementary signal nets exchange charge locally.

To take advantage of the charge redistribution for digital systems, it is mandatory with the present technologies to introduce an extra complementary line with each signal line. This introduction of extra complementary lines results in increased coupling capacitance and increased size of the chip which is undesired. In the case of Deep Sub-Micron (DSM) technology the increase in coupling capacitance results in a significant increase in the total capacitance thereby resulting in undesirable consequences of reduces operation speed and increased power consumption it is therefore, more important in DSM systems to have a charge redistribution system that does not required the addition of complementary signal lines.

Summary of the Invention

The object of this invention is to provide a method and system for reducing power consumption in digital circuits using charge redistribution circuits.

To achieve the said objective, this invention provides a system for reducing power consumption in digital circuits using charge redistribution, comprising:

- a plurality of signal lines;
- an intermediate floating virtual source / sink, and
- a charge redistribution circuit connected to each said signal line that isolates said line from its source and connects it to the intermediate floating virtual source / sink during an idle period prior to a change of state.

The intermediate floating virtual source / sink comprises a charge storage element.

The charge redistribution circuit comprising the transition detector connected to the signal line having two outputs, one of which is connected to the input of a tri-state driver circuit and the other output simultaneously disable the tri-state driver circuit, and enables the control switch to connect its output to the floating source / sink whenever a transition is detected on a signal line.

The charge storage element is a capacitor or a set of capacitors.

The transition detector comprising a delay circuit having its input connected to the signal line and its output connected to the first output of the transition detector and to the first input of a

2-input exclusive-OR or exclusive-NOR gate while the second input of the exclusive-OR/ exclusive-NOR gate is directly connected to the signal line and its output is connected to the second output of the Transition Detector.

The capacitor comprising a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

The invention further provides an integrated circuit for reducing power consumption in digital circuits using charge redistribution, comprising:

- a plurality of signal lines;
- an intermediate floating virtual source / sink, and
- a charge redistribution circuit connected to each said signal line that isolates said line from its source and connects it to the intermediate floating virtual source / sink during an idle period prior to a change of state.

The intermediate floating virtual source / sink comprises a charge storage element.

The charge redistribution circuit comprising the transition detector connected to the signal line having two outputs, one of which is connected to the input of a tri-state driver circuit and the other output simultaneously disable the tri-state driver circuit and enables the control switch to connect its output to the floating source / sink whenever a transition is detected on a signal line.

The charge storage element is a capacitor or a set of capacitors.

The transition detector comprising a delay circuit having its input connected to the signal line and its output connected to the first output of the transition detects and to the first input of a 2-input exclusive-OR or exclusive-NOR gate while the second input of the exclusive-OR/ exclusive-NOR fate is directly connected to the signal line, its output is connected to the second output of the Transition Detector.

The capacitor comprises a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

The present invention also provides a A method for reducing power consumption in digital circuits using charge redistribution, comprising the steps of:

- providing a plurality of signal lines;
- providing an intermediate floating virtual source / sink, and
- isolating each signal line from its source circuit and connecting it to the intermediate floating virtual source / sink during an idle period prior to a change of state.

The step of providing an intermediate floating virtual source / sink comprising supplying a charge storage element.

The change of state is identified by detecting a transition on the signal line.

The charge storage element is supplied by connecting a capacitor or a set of capacitors.

The transition is detected by exclusive-NORing or exclusive-ORing the signal with a delayed version of the signal.

The signal line is connected to the intermediate floating virtual source / sink whenever a transition is detected.

The capacitor is provided by a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

Brief Description of Accompanying Drawings:

The invention will now be described with reference to the accompanying drawings.

Figure 1 shows a system for reducing power consumption in digital circuits using charge redistribution, according to this invention.

Figure 2 shows a system for reducing power consumption in digital circuits using charge redistribution for multiple signal lines.

Figure 3 shows a system for reducing power consumption in digital circuits, having a floating virtual source/sink as mesh and capacitive arrangements.

Figure 4 shows a system for reducing power consumption in digital circuits having a floating virtual source/sink.

Figure 5 shows the block diagram of a charge redistribution cirscuit.

Figure 6 shows the transistion detector used in charge redistribution circuit.

Detailed Description of the Invention:

Figure 1 shows a system for reducing power consumption in digital circuits **100** using charge redistribution for transistion of signal line **101**. The said charge redistribution circuit **102** comprising transition detector and tristate driver including a control switch **103.** The arrangement of transition detector, tristate driver and the switch being such that whenever the signal line **101** undergoes a transition, the charge redistribution ciruit sets the source of the signal line to a high impedence and connects the signal line **101** to the floating virtual source/sink **104** for a period determined by the delay circuit provided in the transition detector of the charge redistribution circuit **102.** RC load **105** is associated with the line **101**.

Figure 2 shows a system for reducing power consumption in digital circuits **200** using charge redistribution circuit **202** in multiple signal lines **201** using floating virtual source/sink **204** extended over all the signal lines. Each signal line **201** is provided with a charge redistribution circuit **202**. The charge redistribution circuit **202** comprises a transition detector, tristate driver and the switch **203.** RC load **205** is assocaited with the line **201.** The arrangement of the said charge redistribution circuit **(202, 203)** and the signal line **201** being such that whenever the signal line **201** undergoes a transition, the charge redistribution circuit sets the source of the signal line to a high impedence and connects the signal lines **201** to the floating virtual source / sink **204** for a period determined by the delay circuit provided in the transition detector of the charge redistribution circuit **202**.

Figure 3 shows a system for reducing power consumption in an integrated digital circuit **300**, having a floating virtual source/sink as mesh **303** and capacitive arrangements **304** as applied

to an integrated digital circuit. Each of the signal lines **301** is connected to a corresponding charge redistribution circuit **302**. In addition, there is a floating mesh **303** connected to the charge redistribution circuits **302**. This mesh **303** is present across multiple subsystems of said integrated digital circuit and may extend across the entire chip.

Initially, the capacitive mesh **303** is discharged, so only (1 to 0) transition injects charge to the mesh. The mesh gradually attains a stable intermediate value and subsequent transitions interact with this intermediate value. In the ideal case, if the intermediate value is VDD/2 then all 1 to 0 going nodes exchange charge till VDD/2 to the floating mesh before drawing power for discharging to the ground. Similarly all 0 to 1 going nodes exhange charge with the floating mesh **303** to reach VDD/2 before drawing power to charge upto the VDD supply.

Figure 4 shows a system for reducing power consumption in digital circuits **400** having a floating virtual source/sink using a conducting mesh **402**, each of the signal lines **401** is connected with an intermediate virtual source/sink **402** through blocks **403**. Blocks **403** detect the transitioning signal line/s **401** and connect them to an intermediate virtual source/sink **402**, before the signal line/s attain/s the desired voltage level.

One of the possible embodiments for detecting and shorting the transitioning signal line (block **403**) may include a transition detector, tristate driver circuit and a switch. The detailed construction of this embodiment is discussed and shown in **figure 5** and **6**.

Figure 5 shows the block diagram of a charge redistribution circuit **500**. A typical charge redistribution circuit comprises a transition detector **501** receiving the signal line as an input **502,** providing a first output **503** and a second output **504** to the tristate driver **505.** The second output **504** of the transition detector **501** is further provided to the control terminal of the control switch **506**. The conducting terminals **507, 508** of the control switch **506** are connected to the output of the tristate driver and to the floating virtual source/sink **509** respectively.

When a signal line **502** undergoes a transition the transition detector **501** provides outputs to enable the tristate driver **505** to set the signal line **502** to a high impedence state and simultaneously enable the control switch **506** to connect the signal line **502** and the floating

virtual source/sink for a predetermined period. The said period for connecting the floating virtual source/sink **509** and signal **502** line is determined by the transition detector.

Figure 6 shows the internal block diagram in the transistion detector **600**. Input signal **601** is delayed by delay circuit **602** and is connected to first input **603** of a 2- input XNOR gate **604** (or XOR gate depending upon the logic used). The delayed signal **603** is further extended as a first output **605** of the transition detector. The second input **606** of the XNOR gate **604** is directly connected to signal line **601**. The output of the XNOR gate **607** is the second output of the transition detector.

When the signal line **601**undergoes a transition due to the delay circuit **602** complementory inputs are received at the inputs **603** and **606** of XNOR gate **604**, resulting in a pulse at the output **607.**

The foregoing description is illustrative of the best mode embodiment of the invention and is not intended to be limiting in any manner. The scope of the invention is defined solely by the accompanying claims.

We claim:

1. A system for reducing power consumption in digital circuits using charge redistribution, comprising:
   - a plurality of signal lines;
   - an intermediate floating virtual source / sink, and
   - a charge redistribution circuit connected to each said signal line that isolates said line from its source and connects it to the intermediate floating virtual source / sink during an idle period prior to a change of state.

2. A system as claimed in claim 1 wherein the intermediate floating virtual source / sink comprises a charge storage element.

3. A system as claimed in claim 1 wherein the charge redistribution circuit comprising the transition detector connected to the signal line having two outputs, one of which is connected to the input of a tri-state driver circuit and the other output simultaneously disable the tri-state driver circuit, and enables the control switch to connect its output to the floating source / sink whenever a transition is detected on a signal line.

4. A system as claimed in claim 2 wherein the charge storage element is a capacitor or a set of capacitors.

5. A system as claimed in claim 3 wherein the transition detector comprising a delay circuit having its input connected to the signal line and its output connected to the first output of the transition detector and to the first input of a 2-input exclusive-OR or exclusive-NOR gate while the second input of the exclusive-OR/ exclusive-NOR gate is directly connected to the signal line and its output is connected to the second output of the Transition Detector.

6. A system as claimed in claim 4 wherein the capacitor comprising a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

7. An integrated circuit for reducing power consumption in digital circuits using charge redistribution, comprising:
   - a plurality of signal lines;
   - an intermediate floating virtual source / sink, and
   - a charge redistribution circuit connected to each said signal line that isolates said line from its source and connects it to the intermediate floating virtual source / sink during an idle period prior to a change of state.

8. An integrated circuit as claimed in claim 7 wherein the intermediate floating virtual source / sink comprises a charge storage element.

9. An integrated circuit as claimed in claim 7 wherein the charge redistribution circuit comprising the transition detector connected to the signal line having two outputs, one of which is connected to the input of a tri-state driver circuit and the other output simultaneously disable the tri-state driver circuit and enables the control switch to connect its output to the floating source / sink whenever a transition is detected on a signal line.

10. An integrated circuit as claimed in claim 8 wherein the charge storage element is a capacitor or a set of capacitors.

11. An integrated circuit as claimed in claim 9 wherein the transition detector comprising a delay circuit having its input connected to the signal line and its output connected to the first output of the transition detects and to the first input of a 2-input exclusive-OR or exclusive-NOR gate while the second input of the exclusive-OR/ exclusive-NOR fate is directly connected to the signal line, its output is connected to the second output of the Transition Detector.

12. An integrated circuit as claimed in claim 10 wherein the capacitor comprises a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

13. A method for reducing power consumption in digital circuits using charge redistribution, comprising the steps of:
   - providing a plurality of signal lines;

- providing an intermediate floating virtual source / sink, and
- isolating each signal line from its source circuit and connecting it to the intermediate floating virtual source / sink during an idle period prior to a change of state.

14. A method as claimed in claim 13 wherein the step of providing an intermediate floating virtual source / sink comprising supplying a charge storage element.

15. A method as claimed in claim 13 wherein the change of state is identified by detecting a transition on the signal line.

16. A method as claimed in claim 14 wherein the charge storage element is supplied by connecting a capacitor or a set of capacitors.

17. A method as claimed in claim 15 wherein the transition is detected by exclusive-NORing or exclusive-ORing the signal with a delayed version of the signal.

18. A method as claimed in claim 15 wherein the signal line is connected to the intermediate floating virtual source / sink whenever a transition is detected.

19. A method as claimed in claim 16 wherein the capacitor is provided by a floating conductor or a floating conducting mesh optionally coupled to capacitor elements.

20. A system for reducing power consumption in digital circuits using charge redistribution substantially as herein described with reference to and as illustrated in the accompanying drawings.

21. An integrated circuit for reducing power consumption in digital circuits using charge redistribution substantially as herein described with reference to and as illustrated in the accompanying drawings.

22. A method for reducing power consumption in digital circuits using charge redistribution substantially as herein described with reference to and as illustrated in the accompanying drawings.

Dated this 30th day of January, 2003

Shanthi Kumar

of **ANAND & ANAND, Advocates**
Agents for the Applicants

ABSTRACT

This invention provides a method and system for reducing power consumption in digital circuits using charge redistribution, comprising a plurality of signal lines, an intermediate floating virtual source / sink, and a charge redistribution circuit connected to each said signal line that isolates said line from its source and connects it to the intermediate floating virtual source / sink during an idle period prior to a change of state.

This charge redistribution provides steady state statistical independent advantage due to charge recycling without inserting extra complimentary line.

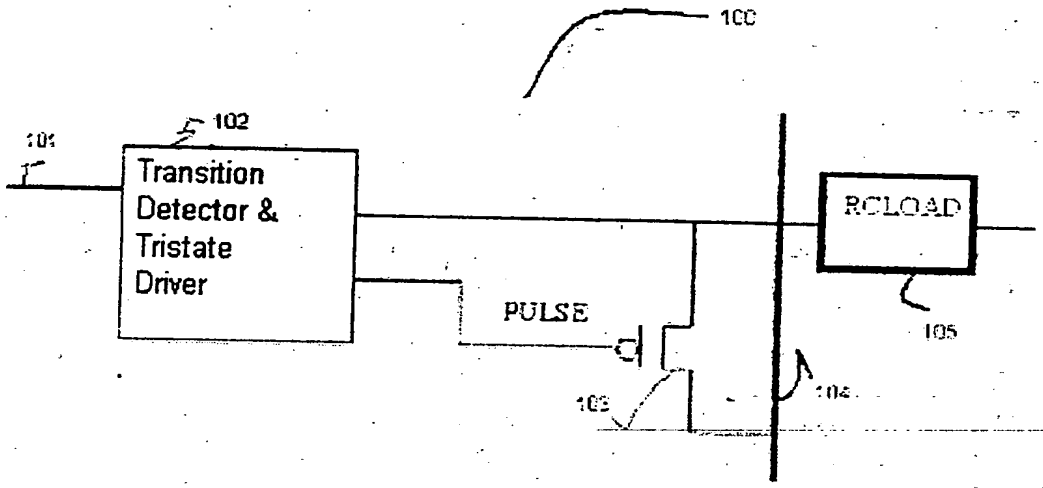

Figure 1

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SHEET 1

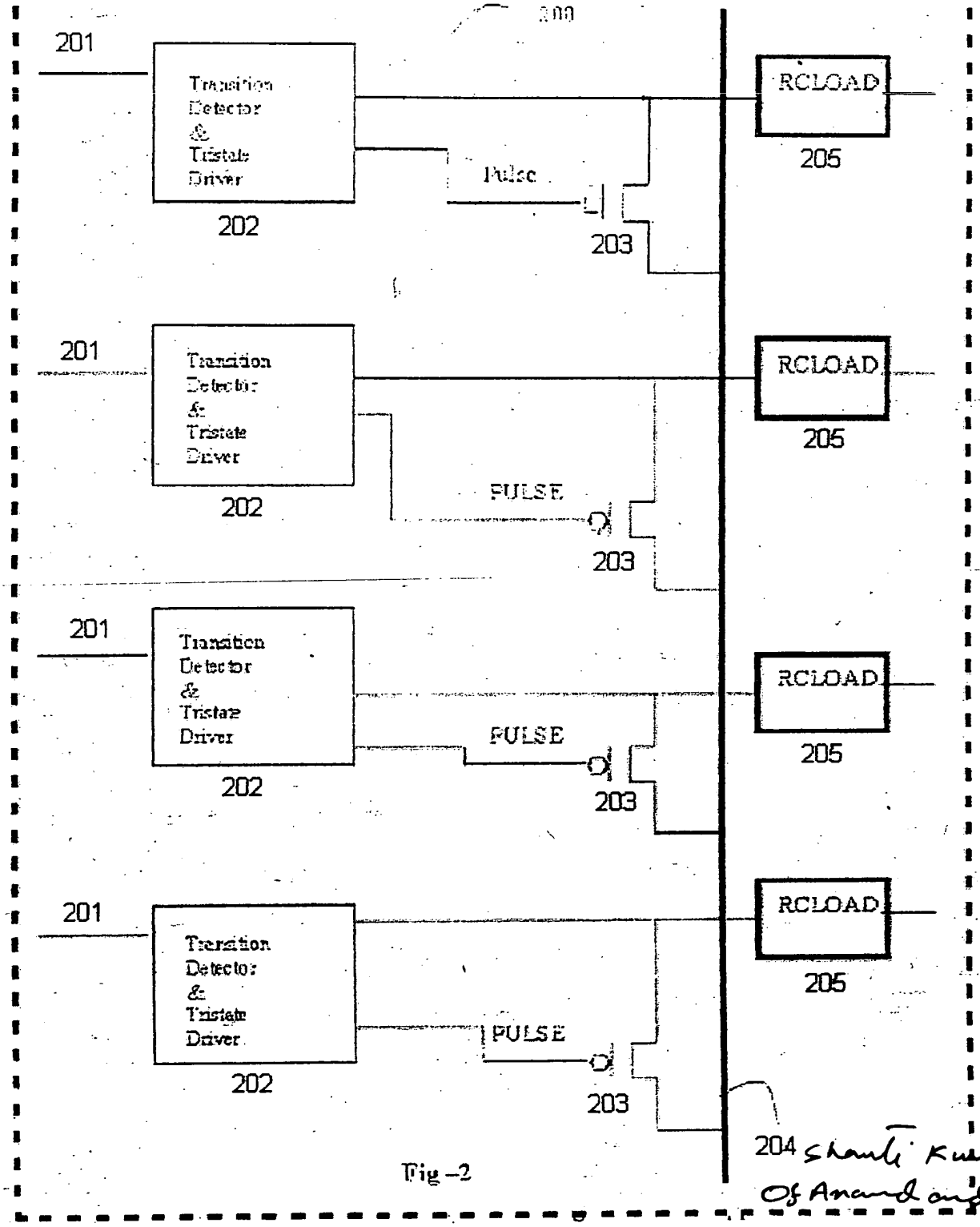

Fig –2

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Advocates
Agents for the Applicants

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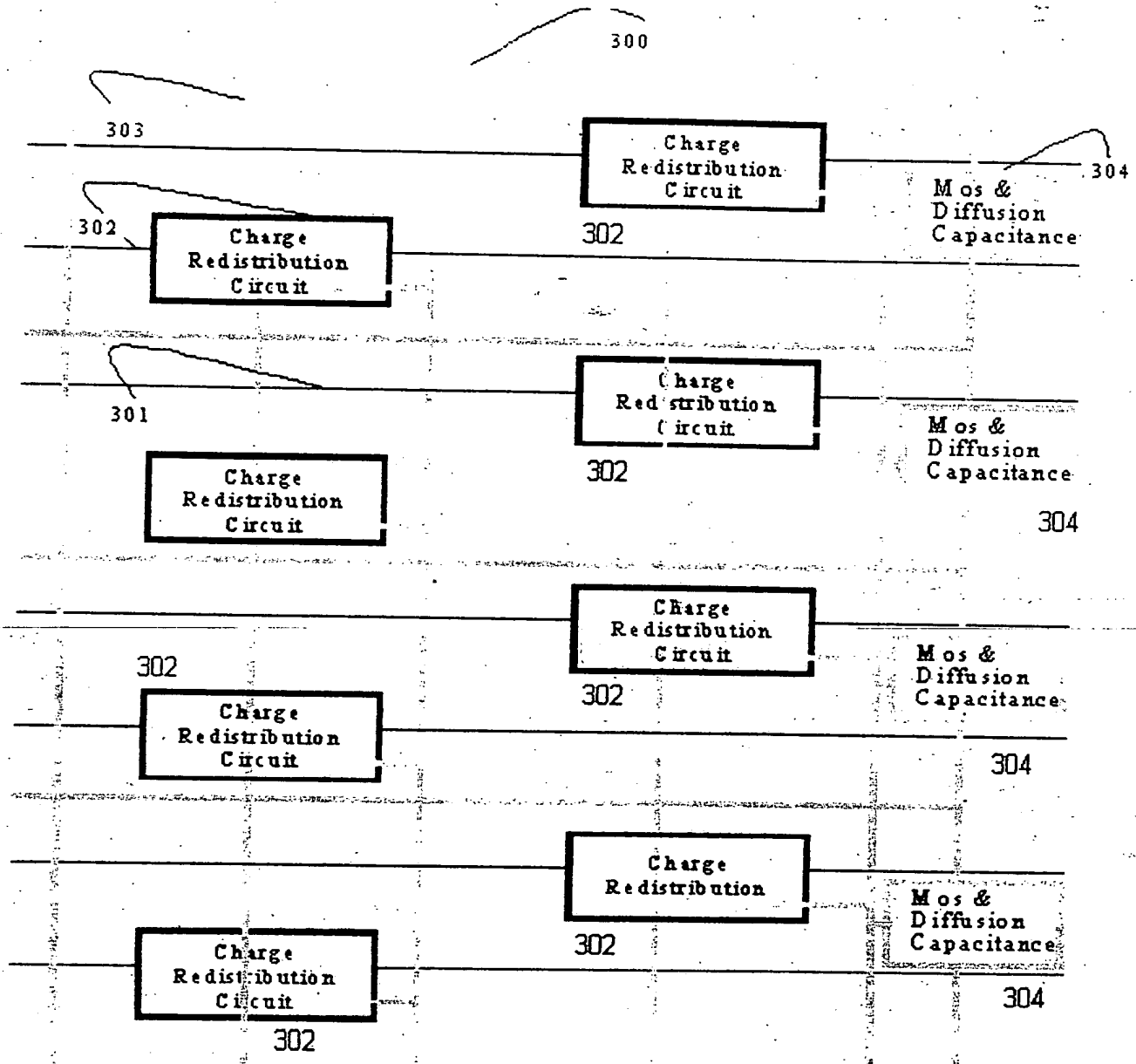
SHEET 3



Floating Mesh DATABUS

Fig - 3

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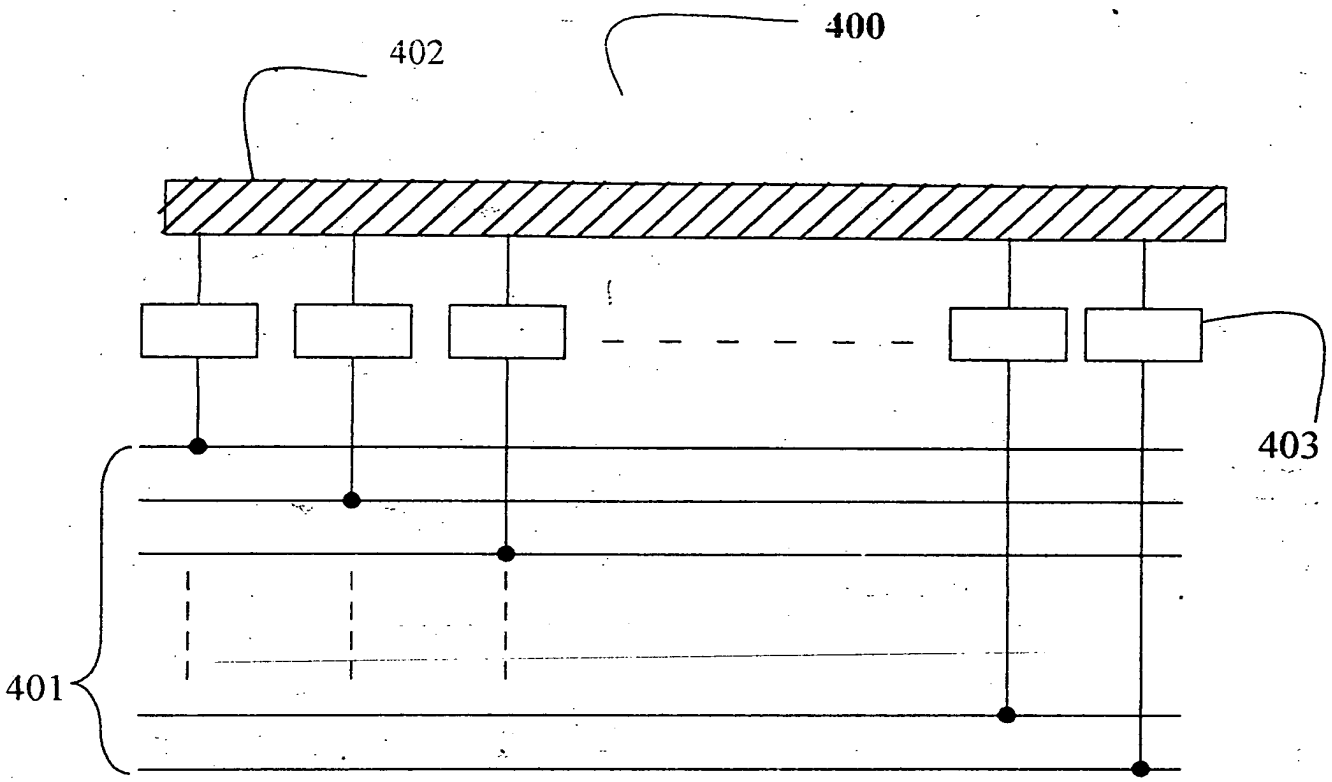

Figure 4

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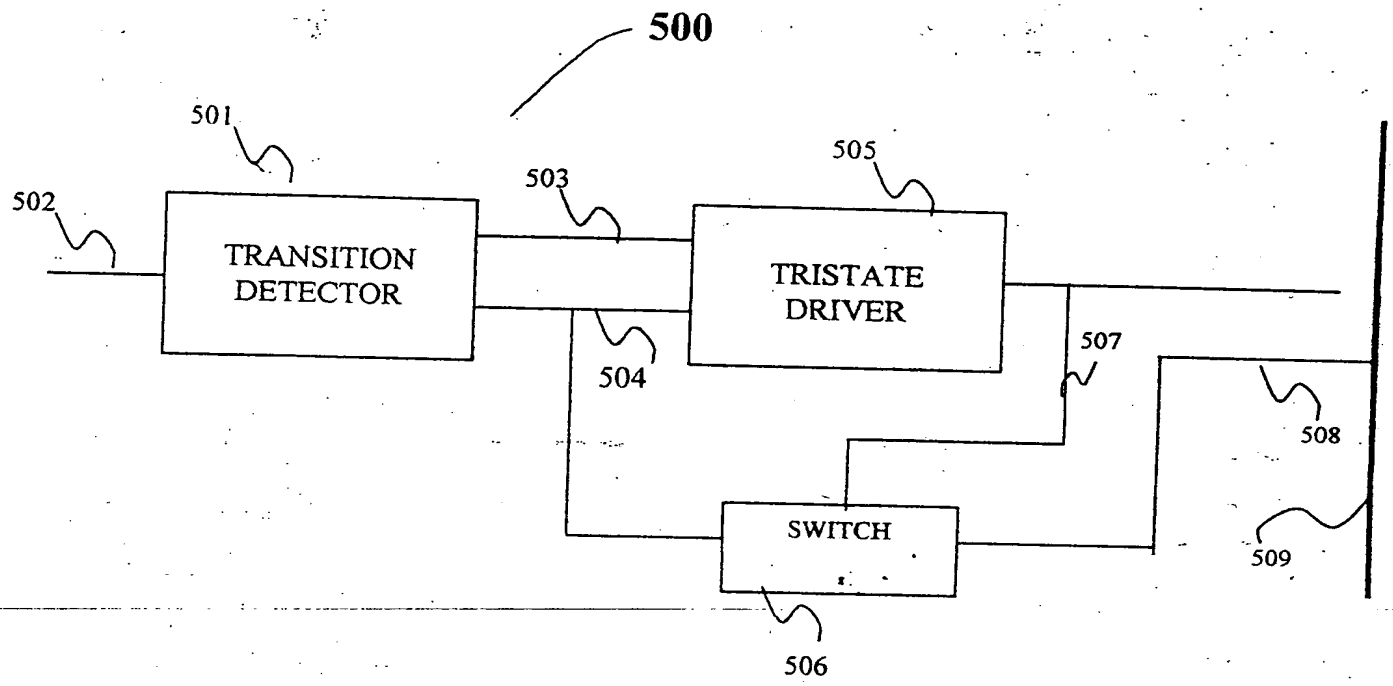

Figure 5
Charge Redistribution Circuit

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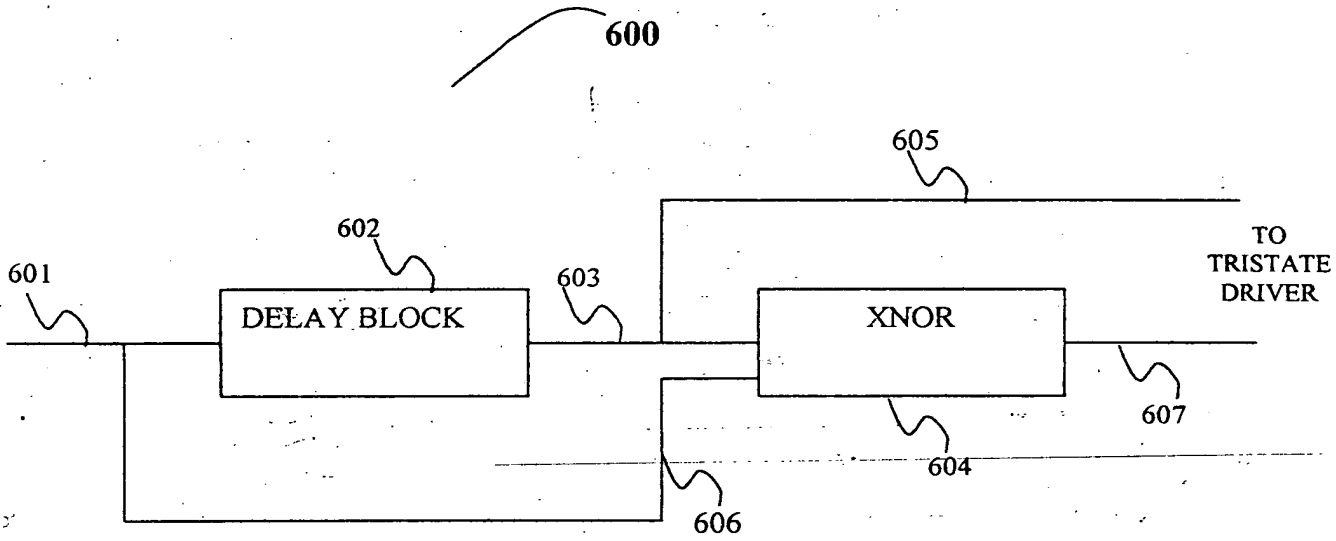

Figure 6
Transition Detector

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